

WHAT IS CLAIMED IS:

1. A high voltage semiconductor device,
comprising:

a drain region disposed within a semiconductor
5 substrate;

a field oxide layer disposed outwardly from the
drain region of the semiconductor substrate; and

a floating ring structure disposed inwardly from at
least a portion of the field oxide layer;

10 wherein a device parameter degradation associated
with the semiconductor device comprises one (1) percent
or less after approximately five hundred (500) seconds of
accelerated lifetime operation.

15 2. The semiconductor device of Claim 1, wherein
the semiconductor device comprises a drain extended metal
oxide semiconductor device.

20 3. The semiconductor device of Claim 1, wherein
the drain region comprises a first dopant type, and
wherein the floating ring structure comprises a second
dopant type approximately complimentary to the first
dopant type.

25 4. The semiconductor device of Claim 1, wherein
the floating ring structure comprises a floating ring
width of no more than forty (40) percent of a field oxide
layer width.

30 5. The semiconductor device of Claim 1, wherein
the floating ring structure is aligned approximately edge
on to an edge of the field oxide layer.

6. The semiconductor device of Claim 1, wherein the floating ring structure is aligned within two levels of misalignment.

5 7. The semiconductor device of Claim 1, wherein the device parameter degradation associated with the semiconductor device comprises one-tenth (0.1) percent or less after approximately five hundred (500) seconds of accelerated lifetime operation.

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8. The semiconductor device of Claim 1, wherein a device parameter associated with the device parameter degradation comprises an on-state resistance.

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9. The semiconductor device of Claim 1, further comprising:

a gate oxide layer disposed outwardly from a semiconductor substrate; and

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a semiconductor gate disposed outwardly from the gate oxide layer;

wherein the semiconductor device operates at a voltage higher than a gate oxide can normally withstand without incurring significant damage.

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10. The semiconductor device of Claim 9, wherein the drain region overlaps approximately thirty (30) to forty-five (45) percent of a semiconductor gate length.

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11. The semiconductor device of Claim 9, wherein the floating ring structure operates to divert at least some current from the gate oxide layer.

12. A method of forming a semiconductor device, comprising:

forming a drain region within a semiconductor substrate;

5 forming a field oxide layer disposed outwardly from the drain region; and

forming a floating ring structure disposed inwardly from at least a portion of the field oxide layer;

10 wherein the floating ring structure comprises a first dopant type that is substantially complimentary to a second dopant type used to form the drain region.

13. The method of Claim 12, wherein the first dopant type comprises primarily a negative-type dopant and the second dopant type comprises primarily a positive-type dopant.

14. The method of Claim 12, wherein the first dopant type comprises primarily a positive-type dopant and the second dopant type comprises primarily a negative-type dopant.

15. The method of Claim 12, wherein forming the field oxide layer comprises a technique selected from a group consisting of local oxidation of silicon and shallow trench isolation.

16. The method of Claim 12, wherein the floating ring structure is aligned approximately edge on to an edge of the field oxide layer.

17. The method of Claim 12, wherein the floating ring structure is aligned within two levels of misalignment.

18. The method of Claim 12, wherein the floating ring structure is formed substantially simultaneously with a channel region of the semiconductor device.

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19. The method of Claim 12, further comprising:

forming a backgate region within the semiconductor substrate; and

10 forming a channel region within the backgate region of the semiconductor substrate, wherein the channel region comprises a substantially similar dopant type as the floating ring structure, and wherein forming the channel region comprises performing a chain implant.

20. A high voltage semiconductor device,
comprising:

a drain region disposed within a semiconductor
substrate;

5 a gate oxide layer disposed outwardly from a
semiconductor substrate;

a field oxide layer disposed outwardly from the
drain region of the semiconductor substrate; and

10 a floating ring structure disposed inwardly from at
least a portion of the field oxide layer and operable to
divert current from the gate oxide layer;

wherein during operation the semiconductor device
operates at a voltage higher than the gate oxide can
normally withstand without incurring significant damage.

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